

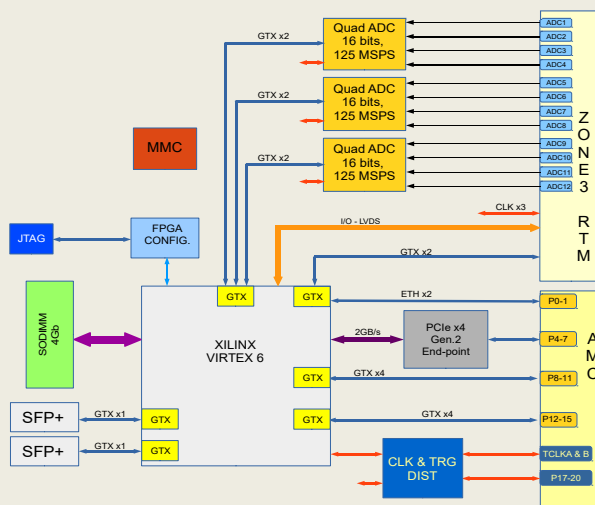
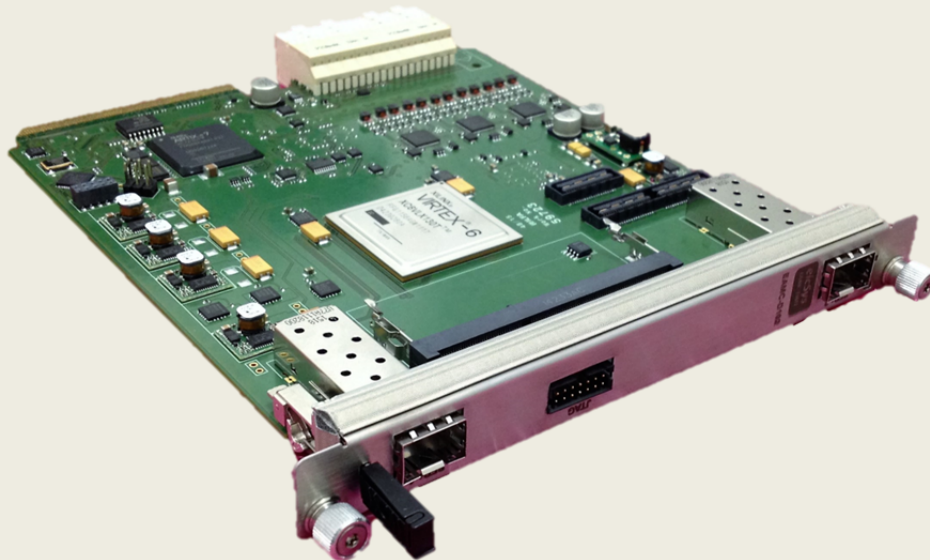
# EAMC-D102 Digitizer Board

## General Description:

The EAMC-D102 is a high speed, high performance 12 ADC (Analog to Digital Converter) Advanced Mezzanine Card (AMC). The module is equipped with programmable, high precision, low jitter clock distribution. The AMC is compliant to MTCA.4 specification and provides 2 x PCIe Gen.2 end-points for redundant operation. The FPGA has an interface to the SODIMM memory (up to 4Gb) and allows for large buffer sizes to be stored during processing. Each ADC input goes to the Rear Transition Module (RTM) connector that complies with uTCA.4. Several boards can be combined into a single multichannel hardware system using fast backplane or fiber links. Provided hardware and software (firmware, drivers, EPICS interface, example applications) accelerate integration of the board into a data acquisition or control system.

**eicSys offers customization of software/firmware according to customer specification.**

## Block diagram:



Specification is subject to change without further notice

Description		
<b>Architecture</b>		
<b>Physical</b>	Dimensions	Double width, mid-size AMC Module Width: 5.486" (148.5 mm) Depth: 7.110" (180.6 mm)
<b>Standards</b>	AMC.0, AMC.1, AMC.2, MTCA.4 Module Management	IPMI version 2.0, MMC V1.0 compatible
<b>Compatibility</b>	Zone3 classification Compatible AMC products	Class D1.0 ERTM-D102
<b>Configuration</b>		
<b>Input/output</b>	Frontpanel	➤ 2x SFP+ ➤ JTAG
	Zone 3	➤ 12 x ADC channels, sampling frequency up 125MHz, 16-bit. ➤ 3 x clock inputs for ADC and FPGA ➤ 2 x MGT interface
	AMC Connector	Ports 0-1 : Ethernet Ports 4-7 : PCIe Gen.2, x4 Ports 8-11 : PCIe Gen.2, x4 in red. system / MGT custom links Ports 12-15 : MGT custom links Ports 17-20 : clock, triggers TCLK_A, TCLK_B, FCLK
<b>Analog signals</b>	ADC	➤ AD9656, 16-bit, 125 Msps ➤ differential AC or DC inputs ➤ 650MHz Full-Power Bandwidth S/H, limited to 150MHz (3dB)
<b>PCIe</b>	2x PCIe x4 Gen. 2	➤ Port 4-7 ➤ Port 8-11
<b>Clock signals</b>	Port 17-20	➤ TCLK B ➤ FCLK ➤ TX/RX
	ZONE 3	➤ TCLK A
<b>Chipset</b>		Virtex6 FPGA
<b>Memory</b>		SODIMM DDR3 memory up to 4GB
<b>Electrical Property</b>		<50 Watt
<b>Software support</b>		Compatible to UniDAQ firmware package firmware upgrade through PCIe
<b>Environmental</b>	Temp. range	Operation: 0°C to +70°C Storage: -40°C to +85°C
	Humidity	5-90%, non-condensing
<b>Ordering Information</b>		<b>EAMC-D102</b>

Datasheet – 11.12.2015, Rev. 1.3

Developed by:  
eicSys Hamburg

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