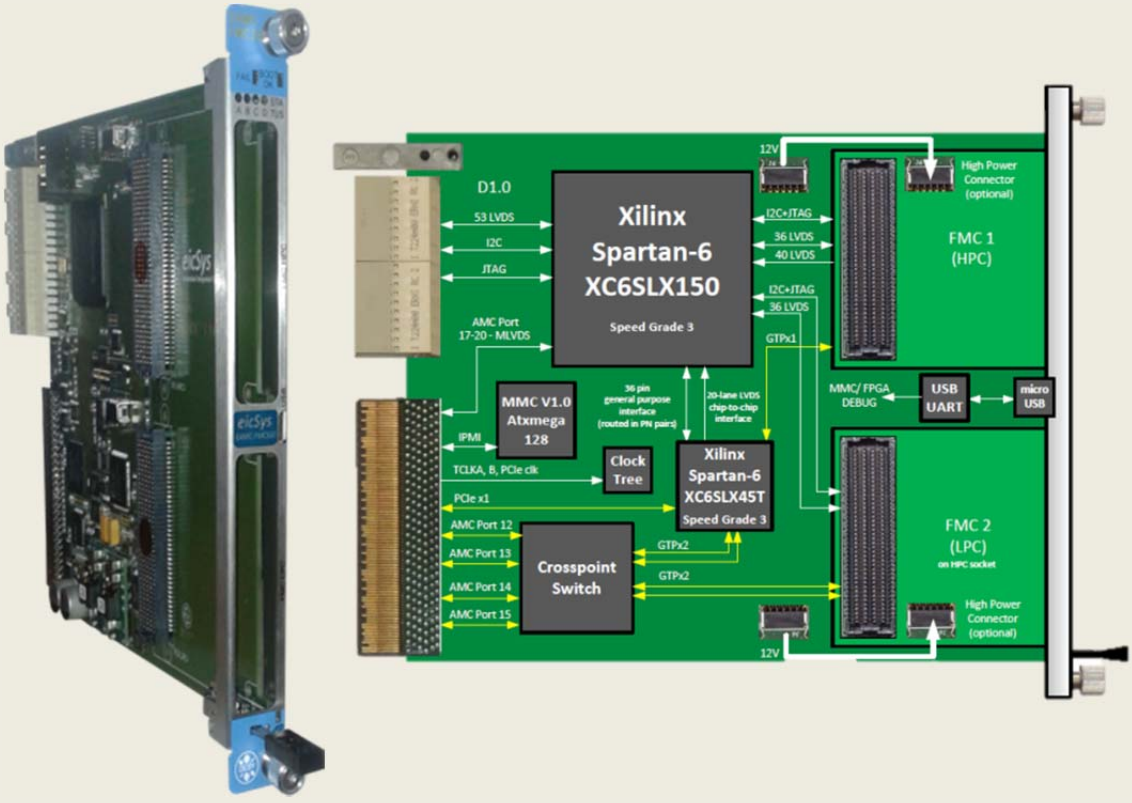
EAMC-FMC500 Dual FMC Carrier

General Description:

The EAMC-FMC500 is developed and licensed by DESY with original part name DAMC-FMC20. It is a cost-efficient FPGA mezzanine card (FMC) carrier designed according to MTCA.4. It is equipped with two Spartan-6 FPGAs.
The carrier simultaneously supports one low pin count and one high pin count FMC module. One FPGA allows serial high-speed communication (PCIe, RTM, Backplane, FMCs). The other FPGA allows implementing large signal processing algorithms. The carrier supports one serial link (GTP) for HPC FMC module and up to two serial links for LPC FMC module. In addition, an extra 12V power connector for high current FMC applications is foreseen for each FMC module. The carrier provides one PCIe link that is AMC.1 type 1 compliant. The carrier is software-reconfigurable over PCIe and MMC. The AMC ports 12-15 are connected via cross-point switch to the transceiver FPGA.
The board is a cost effective approach for basic IO with low computing requirements. An additional USB connection is optional for direct debugging the FPGAs and MMC at the front panel. The carrier management is compliant to the latest recommendation MMC V1.0. The carrier Zone 3 is compliant to the Class D1.0.

Block diagram



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Description			
Architecture			
Physical	Dimensions		Double width, mid-size with full-size option Width: 5.486” (148.5 mm) Depth: 7.110” (180.6 mm)
Standards	AMC.0, AMC.1, AMC.2, MTCA.4 Module management		Advanced Mezzanince Card IPMI version 2.0, MMC V1.0 compatible
Combatibility	Zone3 classification Compatible AMC products		Class D1.0 DRTM-VM2, TBD
Configuration			
Electrical Properties	Power consumption		<50Watt
Chipset	XC6SLX45T, 43,661 logic elements + 4 GTP blocks XC6SLX150, 147,443 logic elements		System FPGA implements external interfaces User FPGA interacts with FMC (HPC+LPC) - transfer rate of 1080 Mb/s per pin can be achived depending on speed grade
Memory	MT45W8MW16BGX 128 Mb		On board RAM
Connectivity			
Frontpanel	FMC Slots	HPC	1 slot
		LPC	1 slot
	Debug interface	Front panel channel, Connector type Data throughput	3 booth FPGAs and MMC Micro USB 3 Mbps
Backplane	Low latency connection	Backplane Connector type Data throughput Bit error rate	up to 2 channels Peer-to-peer, ports 8-15 according to AMC spec. 2.7 or 3.2 Gbps (depending on FPGA) $< 10^{14}$ bit^{-1}
	PCIe	Backplane Connector type Data throughput Bit error rate	1 lanes PCIe gen. 1.0 2.5 Gbps $< 10^{14}$ bit^{-1}
Zone 3	Parallel bus	RTM Connector type Bit error rate	53 differential pairs LVDS $< 10^{14}$ bit^{-1}
	Others	MTCA.4 signals Interlocks JTAG	IPMI bus – I^2C, presence, power supply Dedicated output signals JTAG chain, +3,3V
Other features			
Onboard	RTM management Firmware upgrade Voltage and current monitor Clock monitoring LEDs Mechanical		With power supply and current monitoring Yes, via IPMI and PCIe interface Yes, readout via IPMI Yes, readout via IPMI IPMI management control Hot swap ejector handle
Environmental	Operating temperature Storage temperature Relative humidity Weight		0 – 50°C -40 – 90°C 5 to 90%, non-condensing 0.4 kg

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Developed and licensed by:
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