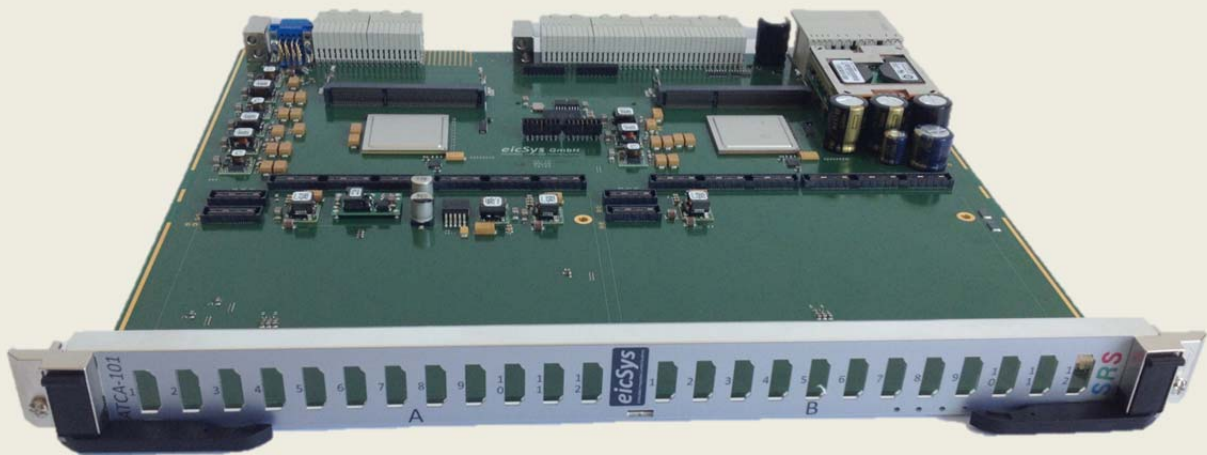


EATCA-101 Carrier Blade

General Description:

The EATCA-101 board is an universal carrier for custom mezzanine modules implemented in ATCA standard. The blade has been designed to optimize the data flow between mezzanines and processing units (2 x Virtex 6 FPGA), the backplane and rear transition modules (RTMs) for a fast, low latency, real time processing. Optional could be used also memory devices (DDR3 SODIMM). The primary application of the blade is trigger and data acquisition system for large scale detectors. The blade provides a high bandwidth, full mesh connectivity for exchanging data between boards in an ATCA crate. For these reasons it can also be used for efficient implementation of control systems - both real time and slow. When supported by ATCA Concentrator Unit it provides huge computation power for digital signal processing. To provide stable, clean clock signals a configurable clock distribution with jitter attenuators is implemented. Read out Systems based on EATCA-101 could be configured for a wide range of data transfers and bandwidth in depend of utilized Mezzanines.

Picture EATCA-101



Specification is subject to change without further notice

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Description		
Architecture		
Physical	Dimensions	288mm x 322mm 8U, 1,2"
Standards	PICMG 3.x ATCA Specification	ATCA Zone 3
Combatibility	ATCA Zone 1 ATCA Zone 2 ATCA Zone 3	ATCA Spec. ATCA Spec. RTM-100, RTM-101
Connectivity		
Blade Interfaces	Frontpanel	USB interface for board programing, diagnostic
	Zone 1	<ul style="list-style-type: none"> ➤ Power <ul style="list-style-type: none"> ○ 80W + up 120W for mezzanine modules ➤ Base interface
	Zone 2	<ul style="list-style-type: none"> ➤ Full-mesh connectivity ➤ P20: clock and trigger signal inputs ➤ 4 x GTX
	Zone 3	<ul style="list-style-type: none"> ➤ 14 x GTX, CLK IN
	Mezzanine	<ul style="list-style-type: none"> ➤ 2 slots for mezzanine, 12V, 60W each
Configuration		
Chipset		2 x Virtex6 LX240T FPGA
Memory		2 x SODIMM DDR2 memory up to 4GB
Mezzanine Interface	<ul style="list-style-type: none"> ➤ 5 banks of data to FPGA: <ul style="list-style-type: none"> ○ 8 x LVDS data lines up to 1GHz DDR ○ 2 x LVDS clock capable pins ➤ 8 x GTX ➤ 1 x clock from the blade (clock distribution) ➤ 16 x single CMOS lines ➤ Power management and board configuration 	
Software support	firmware upgrade through Ethernet or RTM	
Others		
Environmental	Temperature Range	Operation: -40°C to +85°C Storage: -40°C to +90°C
	Humidity	5-90%, non-condensing
	Dimensions	WxH 288mm x 322mm Wight: 0,8Kg
Ordering Information	EATCA-101	

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Developed by:
eicSys Hamburg

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