eicSys GmbH
Embedded Integrated Control Systems

UniDAQ Firmware Package

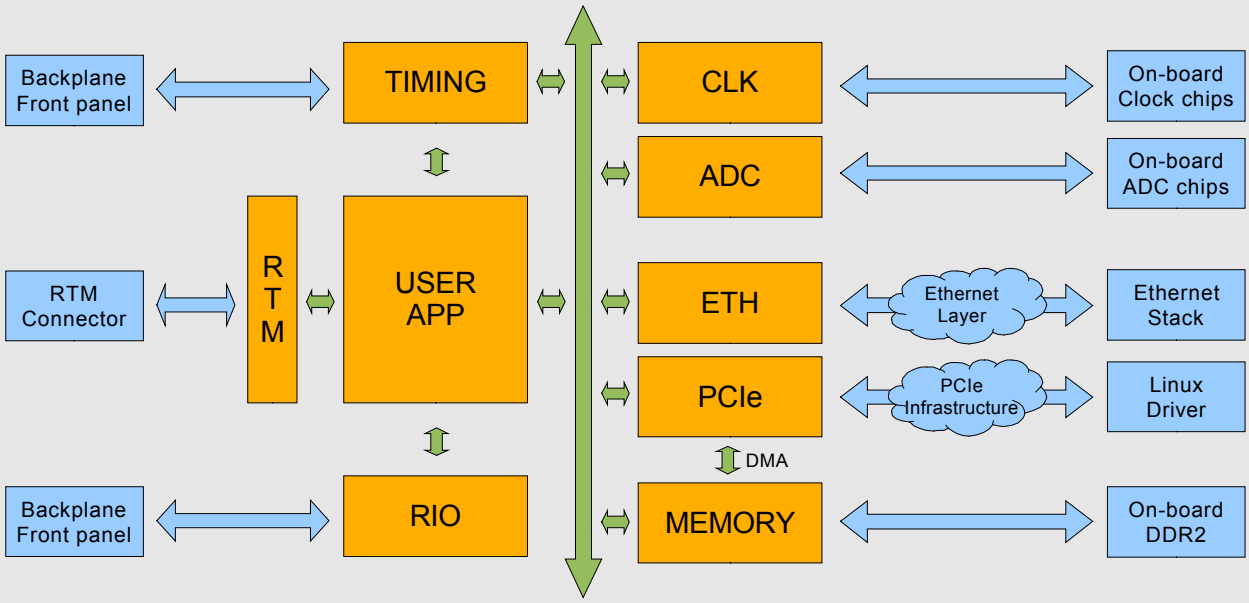
General Description:

The FPGA firmware package dedicated for data acquisition fast ADC boards provides a full support for board components/peripherals, communication channels and acquisition procedures. As part of the package, the simple user application example and an empty template is provided to demonstrate functionality and speed up development process.

Additionally a dedicated Linux Driver is provided. It accommodates DMA functionality, hot-plug support, IRQ based notifications and hardware status reporting.

eicSys company offers customization or extension of selected modules and features according to customer needs. We also offer implementation of a specialized modules based on provided specification.

Block Diagram:



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General Features	
PCIe	x1 to x4 PCIe endpoint accommodates Xilinx Endpoint Block Plus core. It supports 32 bit memory read/write packages and has full DMA support with scatter list implementation. Overall performance of DMA transfer is in range of 830 MB/s. Additionally MSI interrupts and diagnostic registers are supported.
Ethernet	Ethernet module implemented in FPGA fabric provides interface to TEMAC module and implements basic protocol stack up to UDP layer.
Memory	Memory handler compatible with Xilinx MIG (Memory Interface Generator) is provided. For flexibility and performance it is equipped with a configurable 4 port arbiter which allows concurrent access to memory. Memory contents can be accessed by both direct and DMA operations.
RocketIO	For FPGAs equipped with GTP/GTX/GTH gigabit transceivers dedicated protocol handlers and synchronizers have been prepared. They allow fast and flexible transmission among different boards and subsystems.
Clock domain synchronization	Various on-board components require different clocking schemes and they can be clocked using external or internal clock signals. Clock domain synchronization scheme has been prepared to ensure that no data error occur while transmitting signals among modules.
Struck SIS8300 rev. 2 Specific Features	
ADC configuration	Module maps ADCs' serial interface address space into application's address space. This grants easy read/write access to all ADC registers. The module also provides proper synchronization between ADC clock and application clock for incoming data stream.
Clock configuration	Module maps AD9510 serial interface address space into application's address space. This provides easy clocking configuration procedure (selection between front panel and RTM clock, clock delays for individual channels, etc.)
RTM interface	Presented package supports RTM interface which is connected to application modules. Depending on RTM

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	board functionality it can be easily handled with minimal work.
Timing	Module supports external timing interface (trigger, clock) connected via data lines on PORT 17-20 or front panel connector.
Specialized LLRF modules	
IQ detection **IIR filters** **FIR filters**	**Complex number arithmetic** **Non-linearity correctors** **1st and 2nd order interpolators**
Specialized fusion energy modules	
Neutron pulse counting algorithms **Support for high performance switching amplifiers for small signal acquisition**	
FPGA Resource statistics*	
LUT	9552 (33%)
FF	10100 (35%)
BlockRAM	23 (38%)
DSP48	0 (0%)
Target Frequency	125 MHz
* actual resource count may vary depending on sub-module configuration, timing requirements and current firmware version. Includes either ETH or PCIe.	
Ordering Information	UniDAQ.1 – SIS8300
Related Products	UniDAQ.1 – TAMC900
	UniDAQ.1 – EAMC-D102

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